SECTION I. (AMENDMENTS TO THE CLAIMS)

A listing of claims 1-18 of the present application, which are amended and renumbered herein with markings to show changes made, is provided below:

Claims 1-10 (Cancelled).

Claim 11 (Currently amended) An integrated semiconductor structure comprising

a semiconductor substrate comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

at least one PFET and at least one NFET located on the semiconductor substrate, said at least one PFET and said at least one NFET each having a device channel parallel to a surface of said semiconducting substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction, and wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

Claim 12 (Previously Presented) The integrated semiconductor structure of Claim 11 wherein said Group IV semiconducting material is selected from the group consisting of Si, SiGe, SiC, and SiGeC.

Claim 13 (Previously Presented) The integrated semiconductor structure of Claim 12 wherein said Group IV semiconducting material is Si.

Claim 14 (Currently amended) ~~The~~ An integrated semiconductor structure ~~of Claim 11~~ comprising

a semiconductor substrate comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

at least one PFET and at least one NFET located on the semiconductor substrate, said at least one PFET and said at least one NFET each having a device channel parallel to a surface of said semiconducting substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction, and wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.

Claim 15 (Original) The integrated semiconductor structure of Claim 14 wherein the gate dielectric is an oxide.

Claim 16 (Original) The integrated semiconductor structure of Claim 14 wherein the patterned gate conductor comprises polySi.

Claim 17 (Currently amended) The integrated semiconductor structure of Claim ~~11~~ 14 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

Claim 18 (Cancelled)